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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,006	02/16/2001	Aaron Schoenfeld	303.259US3	5063

7590 07/17/2006

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,006	SCHOENFELD, AARON	
	Examiner	Art Unit	
	Evan Pert	2826	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25,35-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25,35-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-25, 35-39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over INTEGRATED CIRCUITS – Design Principles and Fabrication (1965 textbook) taken with DEVICE ELECTRONICS for INTEGRATED CIRCUITS (1986 textbook), in view of Yamada (US 5,266,528), (along with US 5,408,739 [col. 6, lines 55-60] relied on for teaching of a Universal Fact).

The 1965 and 1986 textbooks show what is known as a "semiconductor die", which is a rectangular area to be cut from a processed semiconductor wafer to form a chip [see Figs. 5-43, 5-14 and 5-13 of the 1965 text and also see Figure 2.1 of the 1986 text].

As seen in Fig. 5-43 of the 1965 text, a rectangular semiconductor die has active circuitry in a "first region" which is "surrounded by an unused blank second region" on a "first planar surface" (see Figs. 5-13 and 5-14), has an opposing second planar surface, and is separated along lanes surrounding the die as seen in fig. 5-43, creating a rectangular semiconductor die with "perimeter side surfaces". The rectangular semiconductor die also has metallization (i.e. "metal features") that are located near the "perimeter side surfaces" (see Figs. 5-13 and 5-14).

In the 1965 text, the separation occurs by scribing and breaking, which gives rough edges as seen for the 1964 chip of Fig. 2.1 of the 1986 text; yet, improvements in separation of dice have led to smoother perimeter side surfaces as seen for the 1970 chip in Fig. 2.1.

Yamada US 5,266,528 shows a chip separation improvement where chips are ground away from the wafer with saw blades at the lanes like the lanes seen in Fig. 5-43 of the 1965 text.

When one adopts the Yamada method of chip separation, a cut with "resin blade" results in a smooth, effectively polished surface, as explained in US 5,408,739: "A resin blade is well known in the art of semiconductor dicing and can provide a high quality surface which does not need further processing, such as polishing," which means that the cut with a "resin blade" in Yamada is so smooth, that the cut surface can be considered as "polished."

When one adopts the Yamada method, the side perimeter surfaces of the cut chip may have two offset surfaces from the grinding/polishing cuts [i.e. when the second cut with resin blade is narrower than the blade of the first cut], or may have a planar, effectively polished, perimeter side surface extending from the top side of the chip to the backside of the chip [i.e. when the second blade cut is the same width as the first cut].

The 1965 text explains that "minimum die size" should be maintained [summary point 8 at p. 162], as is repeated throughout the prior art, such as cited in earlier rejections. This means that the ordinary of skill in the art know that the spacing in Fig 5-43 from an "edge metal feature" (e.g. die bond pads) to the cut perimeter side surface should be as small as possible, the distance decreasing with increasing precision in cutting as seen in Fig. 2-1 of the 1986 text.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt the dice separation method of Yamada for separating dice from a wafer like the dice shown in Fig. 5-43 of the 1965 text and Fig. 2.1 of the 1986 text.

One of ordinary skill in the art would have been motivated to adopt the improved chip separation of Yamada "to suppress the occurrence of cracks during dicing in the production of semiconductor chips" [col. 2, lines 22-24].

Furthermore, in adopting the cutting method of Yamada, one of ordinary skill in the art would be motivated to minimize die size (e.g. at the direction of the 1965 text), such that the distance of bond pads to the chip edge would be as small as possible such as "less than 5 um." In adopting the resin blade at a smaller thickness or the same thickness as the first cut by Yamada, the resultant die would have a very smooth, effectively polished surface at every resin blade cut.

Furthermore, the RCE-added-limitation of "an edge metal feature" being "less than 5 microns" from the chip edge is just a recitation of an obvious change of size/shape of the prior art. Likewise, recitation of "polished" characterizing the side surfaces of the die is just an obvious change in shape of prior art, with nothing unexpected. The courts have held that recitation of prior art with changes only to size/shape is not patentable unless there is some unexpected result [see MPEP 2144.04(IV)]. There is no size or shape change of prior art in this case that results in anything "unexpected."

Response to Arguments

2. There is nothing unexpected about the "die" that applicant is claiming, with stepped edge or straight edge, and about 5 microns or less blank space between die edge(s) and bond pads of circuitry on the die. Even though the claimed die includes a RESULT of the process already patented to applicant where a die is originally cut bigger than desired with rough edges, and then polished down to size, wasting wafer material, the product RESULT is not patentable because the result is an obvious "semiconductor die" in view of prior art. Once a "semiconductor die" has been ground and/or polished to the desired size in applicant's already-patented method invention, the die can not be distinguished from prior art dice that are carefully and painstakingly cut (i.e. less efficiently) with better saw blade methods.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ETP
July 9, 2006

EVAN PERT
PRIMARY EXAMINER